

**SUMMARY**

The Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@novakov.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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## APPENDIX A

### ABSTRACT OF THE DISCLOSURE

~~A phase-locked loop (PLL) frequency synthesizer comprising: 1) a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency,  $F_{out}$ , determined by the frequency control voltage level; 2) a first frequency divider for dividing the operating frequency,  $F_{out}$ , of the output clock signal by a first divider value,  $N$ , to produce a first divided clock signal having a frequency,  $F_{out}/N$ ; 3) a second frequency divider for dividing a reference frequency,  $F_{in}$ , of an incoming reference clock signal by a second divider value,  $M$ , to produce a second divided clock signal having a frequency,  $F_{in}/M$ ; and 4) a phase-frequency detector for comparing the first and second divided clock signals and generating an UP control signal if the first divided clock signal is slower than the second divided clock signal and generating a DOWN control signal if the first divided clock signal is faster than the second divided clock signal. The PLL frequency synthesizer further comprises: 5) a charge pump for receiving the UP and DOWN control signals and increasing the frequency control voltage level on the loop filter by injecting a charge pump current,  $I_C$ , and decreasing the frequency control voltage level on the loop filter by draining the charge pump current,  $I_C$ ; and 6) a loop response control circuit for adjusting a value of  $I_C$  as a function of the first divider value,  $N$ , and the second divider value,  $M$ .~~ A (PLL) frequency synthesizer comprising: 1) a VCO that generates a first clock having frequency,  $F_{out}$ , determined by a loop filter control voltage; 2) a first divider for

dividing Fout by N to produce a second clock of frequency, Fout/N; 3) a second divider for dividing a reference frequency, Fin, by M to produce a third clock of frequency, Fin/M; 4) a phase-frequency detector for comparing the second and third clocks, generating an UP signal if the second clock is slower than the third clock, and generating a DOWN signal if the second clock is faster than the third clock; 5) a charge pump that receives the UP and DOWN signals and increases or decreases the control voltage on the loop filter by injecting or draining a charge pump current, Ic; and 6) a loop response control circuit for adjusting Ic as a function of N and M.

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PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER USING  
AUTOMATIC LOOP CONTROL AND METHOD OF OPERATION

## ABSTRACT OF THE DISCLOSURE

5

A (PLL) frequency synthesizer comprising: 1) a VCO that generates a first clock having frequency,  $F_{out}$ , determined by a loop filter control voltage; 2) a first divider for dividing  $F_{out}$  by  $N$  to produce a second clock of frequency,  $F_{out}/N$ ; 3) a second divider for dividing a reference frequency,  $F_{in}$ , by  $M$  to produce a third clock of frequency,  $F_{in}/M$ ; 4) a phase-frequency detector for comparing the second and third clocks, generating an UP signal if the second clock is slower than the third clock, and generating a DOWN signal if the second clock is faster than the third clock; 5) a charge pump that receives the UP and DOWN signals and increases or decreases the control voltage on the loop filter by injecting or draining a charge pump current,  $I_c$ ; and 6) a loop response control circuit for adjusting  $I_c$  as a function of  $N$  and  $M$ .